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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,054	11/15/2001	Byoung W. Min	SC11721TP	4428

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MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,054	MIN, BYOUNG W.	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-10 and 12-17 in Paper No. 6 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 9, 10, 12-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in combination with Rutten et al. ('293).

Matsumoto discloses a prior art method of forming contacts for semiconductor devices which includes providing silicon-on-insulator (SOI) semiconductor stack comprised of active layer 3 formed over first insulator layer 2 wherein the first insulator layer is formed over semiconductor substrate 1 (Col. 1, lines 45-48), then etching a portion of active layer 3 to form a trench opening (Col. 1, lines 62-64), subsequently forming second insulator layer 4 within trench opening adjacent to active layer 3 and on first insulator layer 2 (Col. 1, lines 64-65, and Fig. 3B), then performing p-type dopant implant through second insulator layer 4, first insulator layer 2 and active layer 3 to form first doped region 5 within semiconductor substrate 1 (Col. 1, lines 66-67, and Fig. 3B), then forming gate dielectric layer 6 on the surface of active layer 3 (Col. 2,

lines 1-3, and Fig. 3C), forming gate electrode 7 on gate dielectric layer 6 (Col. 2, lines 3-4), subsequently forming source and drain regions 8 in active layer 3 at each side of gate electrode 7 thereby forming a channel region underneath gate electrode 7 (Col. 2, lines 4-7), subsequently forming interlayer dielectric layer 9 over second insulator layer 4 and active layer 3 (Col. 2, lines 8-10, and Fig. 4A), then forming contact hole 10 by etching through interlayer dielectric layer 9, second insulator layer 4 and first insulator layer 2 (Fig. 4A), then forming second contact holes 10 by etching through interlayer dielectric layer 9 thereby contacting source and drain regions 8 in active layer 3 (Fig. 4A).

Matsumoto's prior art does not disclose filling contact holes with conductive material such as metal to form contact electrically connected to first doped region and source and drain regions.

Matsumoto discloses forming contacts for semiconductor devices on silicon-on-insulator (SOI) semiconductor stack with contact holes 10 which are then filled with conductive materials to form conductive plugs (Col. 6, lines 5-9).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation of contact holes 10 to be performed.

Matsumoto's prior art does not disclose that the conductive material is comprised of metal.

Rutten et al. teaches a method of forming conductive contact holes to provide electrical interconnection in semiconductor devices by etching through first and second insulating layers 14 and 3 and interlayer dielectric layer 4, and then filling trench 11 with conductive material such as metal (Col. 7, lines 36-42, and Fig. 4).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Rutten et al. with the combination because it would enable formation of contact holes 10 of the combination to be performed and obtain further advantage of reducing additional silicon area (Col. 4, lines 5-7).

4. Claims 7, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto ('562) in combination with Rutten et al. ('293) as applied to claims 1-6, 9, 10, 12-14 and 16-17 above.

The combination process does not disclose that the p-type dopant is boron.

Rutten et al. discloses that a typical p-type dopant for implanting includes boron (Col. 6, lines 20-21).

It would have been within the scope to one ordinary skill in the art to combine the teachings because it would enable the step of performing p-type dopant implant of Matsumoto's prior art to be performed.

In regard to claims 8 and 15, the choice of doping energy would have been a matter of routine optimization to achieve the desired device dimensions and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

November 3, 2002

George Fourson
Primary Examiner
Art Unit 2823